NS8803 Datasheet

Version 1.4

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NSING Technologies Inc.

Critical Features

- **Bluetooth 5.1 Low Energy Technology**

- Full Feature Set BLE 5.1 Subsystem
- Advertising Extensions
- Angle of Arrival/Departure
- AES-128 Hardware Acceleration
- Up to 10 Concurrent Links
- Simultaneously Master and Slave Role
- Dual Peripheral Option
- Wi-Fi Coexistence

- **Low Power**

- DCDC Regulation. Wide Supply Voltage Range: 1.62V - 3.63V
- Rx Current: 3mA@3V
- Tx Current @ 0 dBm: 3mA@3V
- Retention LDO for Low Power Sleep Mode. Sleep Mode Current: 1μA
- Shutdown Current: 100nA

- **High Performance RF Transceiver**

- 2.4GHz RF Transceiver Compliant to BLE 5.1 Specification
- Excellent Rx Sensitivity (-96dBm), Selectivity and Blocking Performance
- Programmable Tx Output Power up to +6dBm
- Integrated Antenna Matching Network

- **Build in 32-bit Processor**

- ARM CM0 Processor, Clock Speed up to 32MHz
- 256kB Embedded Flash
- 64kB RAM
- SPI Slave, SPI Master, I2C, UART, Timers, WDT, PWM, GPADC, GPIOs

- **Clocks**

- 32MHz XTAL
- 32.768kHz XTAL
- 32MHz RC Oscillator
- 32kHz RC Oscillator

- **Data Interface**

- Standard HCI (UART/SPI) under BLE controller setup

- **Process**

- TSMC 40nm ULP
- Metal stack: 5X1Z1U (1P8M) + AP_RDL

Table of content

VERSION

Version No.	History	Author	Date
V0.0	Created	NSING	2016-09-26
V0.1	Add DAOUT and TXEN PIN	NSING	2016-10-26
V0.2	Add DCDC_FLAG/ VDDC_FLAG/ DCDC_REQ/ BLE_IRQ signals and description. Update illustrated.	NSING	2016-11-08
V0.3	Add B2M_STATEVLD/CLK32k/SWD signals and description. Modify B2M_STATE[2:0] define. Add Bonding diagram. Modify figure1,2,3,15. Modify table 2,3,4,9.	NSING	2016-11-24
V0.4	Modify SWD TESTPAD[14:0] signals, add SWDOEN. Modify figure 2,3,9,10	NSING	2016-12-02
V0.5	Modify figure1, figuer12, table 2,3,10 Add Table 3's note Add TESTPAD[20:15] signals	NSING	2017-1-12
V0.6	Modify table 3, chapter 11, Figure 1,5,6 Add TESTPAD2~10 configure requirement. Modify SPI_STATUS/BLE_IRQ description. Modify communication flow, add controller sent to host flow.	NSING	2017-2-16
V0.7	Modify Figure 6, table2; add chapter 11	NSING	2017-4-28
V0.8	Modify Table 10, add SPIS IO multiplexing	NSING	2017-6-23

	description for SPI download mode。 Modify Figure 6, add 7)		
V0.9	Modify Figure 13, Figure 14	NSING	2017-07-24
V0.10	Modify Table 3: TESTPADx default value Modify Table 10, add UART_RXD/TXD	NSING	2017-08-22
V0.11	Modify Figure 1: add DVDD and VSSGR Modify Table 2 and 3	NSING	2017-09-29
V1.0	Modify version to 1.0	NSING	2017-10-12
V1.1	Updated for NS8803 design	NSING	2020-04-25
V1.2	1. Update specifications 2. Add clocking section	NSING	2020-05-12
V1.3	Update board connection	NSING	2020-05-13
V1.4	Add NS8803 pads	NSING	2020-05-14

1. Block diagram

NS8803 incorporates BLE 5.1 compatible 2.4GHz RF transceiver, modem, baseband and 32bit link layer processor. There are both crystal and RC oscillators designed on chip. The crystal circuits can also take single-ended clock from other chip or external clock sources. 32MHz crystal clock is the frequency reference for the radio and also serves as the main clock source for the other building blocks such as modem, baseband, etc. Bluetooth low energy requires a low speed clock with better than ±500ppm accuracy if the device is to go to sleep mode while advertising or maintaining connection(s). For normal use case, the 32.768kHz crystal provides this sleep clock. However, in some use cases the internal 32kHz RC oscillator can be compensated to meet the clock accuracy requirements. 32.768kHz crystal can be eliminated in this case. The internal high-speed oscillator (RC 32MHz) can be used as a clock source for the link layer processor before crystal clock is stable. 256kB EFlash and 64kB RAM are integrated internally with 32kB RAM as a dedicated memory for link layer processor. SPI is used as the default interface to the external host MCU.

Below shows the block diagram of NS8803.

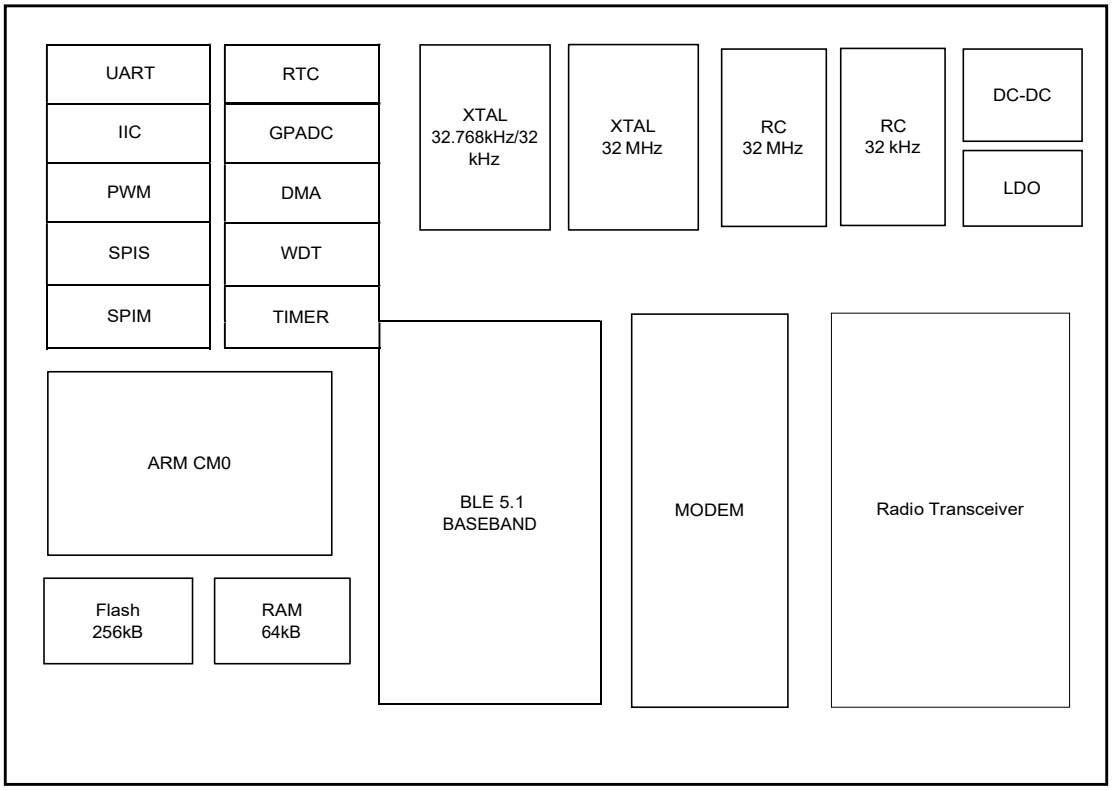

Figure 1: NS8803 block diagram

2. Process

Table 1: NS8803 process list

	Description	Note
Process	TSMC 40 NM CMOS MIXED SIGNAL RF ULTRA LOW POWER 1P10M+AL_RDL SALICIDE CU_ELK 0.9/2.5V PDK	Cadence OA
Metal	1P8M（5X1Z1U）+ AP-RDL	
Mask	50	
Area	2241um * 1906.2um	post shrink, including seal ring, without scribe line

3. Pads

Table 2: NS8803 Pads

NO.	Pad Name	Note
1	GPIO17_PAD	Multiplex with SWCLK and ANATEST1
2	GPIO16_PAD	Multiplex with SWDIO and ANATEST0
3	GPIO15_PAD	GPIO
4	VCCESD	ESD supply
5	VSSESD	ESD ground
6	UARTRXD_PAD	UART RX
7	UARTRTS_PAD	UART RTS
8	UARTCTS_PAD	UART CTS
9	UARTTXD_PAD	UART TXD
10	VSSESD	ESD ground
11	VCCESD	ESD supply
12	DVDD	NS8803 digital supply
13	VSSD	NS8803 digital ground
14	VCC	Chip supply
15	VSSESD	ESD ground
16	SPISMOSI_PAD	SPI slave MOSI
17	SPISMISO_PAD	SPI slave MISO
18	SPISCLK_PAD	SPI slave CLK
19	VSSA	NS8803 analog ground
20	VDCDCRF	DC-DC output for radio LDOs supply
21	VDCDCRF	DC-DC output for radio LDOs supply
22	VDDPA	Power amplifier supply
23	RFIOM	RF Front-end ground
24	RFIOM	RF Front-end ground
25	RFIOP	Antenna port
26	RFIOP	Antenna port
27	RFSUB	RF substrate ground
28	VCCESD	ESD supply
29	VSSESD	ESD ground
30	TXEN	Transmitter enable/disable, high active
31	VSSGR	RF guard ring ground
32	VSSVCO	VCO ground
33	VSSESD	ESD ground
34	VCCESD	ESD supply
35	VCCESD	ESD supply
36	VSSESD	ESD ground

37	VSSS	RF substrate ground
38	XO32MM	32M crystal port
39	XO32MP	32M crystal port
40	VSSESD	ESD ground
41	VSSP	DC-DC ground
42	VSSP	DC-DC ground
43	SWITCH	DC-DC output
44	SWITCH	DC-DC output
45	RESETN	NS8803 power down control, low active
46	VCCESD	ESD supply
47	VSSESD	ESD ground
48	VDCDC	DC-DC output for digital LDO supply
49	GPIO14_PAD	GPIO
50	SPIMCSN_PAD	SPI master CSN
51	SPIMMISO_PAD	SPI master MISO
52	SPIMMOSI_PAD	SPI master MOSI
53	SPIMCLK_PAD	SPI master CLK
54	VSSESD	ESD ground
55	SPISCSN_PAD	SPI slave CSN
56	STATUS_PAD	NS8803 operation status, L: sleep or power down, H: Waken up
57	SPIS_IRQ_PAD	SPI slave IRQ
58	CLKREQ_PAD	CLK request for single-ended clock sourcing case
59	CLKACK_PAD	CLK acknowledgement from MCU
60	VSSD	Digital ground
61	VCCESD	ESD supply
62	XO32kM	32.768kHz crystal port
63	XO32kP	32.768kHz crystal port
64	VSSESD	ESD ground
65	WLAN_PTI_1_PAD	Wi-Fi coexistence pad, WLAN Packet Traffic Information
66	WLAN_PTI_2_PAD	Wi-Fi coexistence pad, WLAN Packet Traffic Information
67	XO32MP_test	32MHz single-ended clock input
68	WLAN_TOG_PAD	Wi-Fi coexistence pad, WLAN Packet Traffic Information Qualifier
69	WLAN_PTI_0_PAD	Wi-Fi coexistence pad, WLAN Packet Traffic Information
70	WLAN_PTI_3_PAD	Wi-Fi coexistence pad, WLAN Packet Traffic Information
71	VSSESD	ESD ground
72	WLAN_RX_ABORT_PAD	Wi-Fi coexistence pad, WLAN Reception Abort Request

73	WLAN_TX_ABORT_PAD	Wi-Fi coexistence pad, WLAN Transmission Abort Request
74	WLAN_RX_PAD	Wi-Fi coexistence pad, WLAN Reception On-going
75	VCCESD	ESD supply
76	WLAN_TX_PAD	Wi-Fi coexistence pad, WLAN Transmission On-going
77	VSSESD	ESD ground
78	CMS0_PAD	Chip mode control
79	VPP	Medium voltage pin used in flash test mode
80	CMS1_PAD	Chip mode control
81	ANATEST1	Analog test port 1
82	ANATEST0	Analog test port 0
83	VSSD	Digital ground
84	VSSESD	ESD ground
85	SCL_PAD	IIC clock
86	SDA_PAD	IIC data IO

4. Specifications

4.1 Absolute Maximum Ratings

Table 3: NS8803 Operating Condition

Parameter	Min	Typ	Max	Unit	Note
Operation Temperature	-40	+25	+85	℃	Ambient
Storage Temperature	-40	+25	+150	℃	
MSL			1		
ESD HBM			+/-4000	V	
ESD CDM			+/-500	V	
Voltage of VCC	1.62	3	3.63	V	
$V_{I/O}$	-0.3		3.63	V	
RFIO Input Power			+10	dBm	
Flash Endurance	10000			Cycles	Write/Erase
Flash Retention	10			Years	125℃

4.2 Electrical Specification

Measured with T_c = 25℃, VCC = 3V and f_{RF} = 2440MHz, unless otherwise noted.

Table 4: NS8803 Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Note
Power Consumption						
I_Active Rx	Radio Rx current		3.0		mA	
I_Active Tx	Radio Tx current @ 0dBm		3.0		mA	
I_Idle	Idle mode current		TBD		uA	
I_Standby	Standby mode current		TBD		uA	
I_Sleep	Sleep mode current		1		uA	

I_Reset	Reset IO mode current		0.1		uA	
RF						
RF_{IMP}	RFIO Impedance		50		ohm	
AC Characteristics - Rx						
P_{SENS}	Receiver Sensitivity		-96		dBm	1 Mbps BLE ideal transmitter, <=37 bytes, PER < 30.8%
			-93		dBm	2 Mbps BLE ideal transmitter, <=37 bytes, PER < 30.8%
$P_{SENS, VAR}$	Rx sensitivity variance between channels		+/- 0.5		dB	
$P_{RX, MAX}$	Maximum receiver input power level			+10	dBm	1/2 Mbps BLE ideal transmitter, <=37 bytes, PER < 30.8%
$C/I_{co\text{-}channel}$	Co-Channel interference		7		dB	Wanted signal at –67dBm, modulated interferer in channel, PER < 30.8%
$C/I_{+/-1MHz}$	+/-1MHz Channel interference		-4		dB	Wanted signal at –67dBm, modulated interferer in channel, PER < 30.8%
$C/I_{+/-2MHz}$	+/-2MHz Channel interference		-33		dB	Wanted signal at –67dBm, modulated interferer in channel, PER < 30.8%
$C/I_{+/-3MHz}$	+/-3MHz Channel interference		-44		dB	Wanted signal at –67dBm, modulated interferer in channel, PER < 30.8%

C/I_{image}	Image Channel interference		-29		dB	Wanted signal at –67dBm, modulated interferer in channel, PER < 30.8%
$C/I_{image+/-1MHz}$	Image Channel +/-1MHz interference		-37		dB	Wanted signal at –67dBm, modulated interferer in channel, PER < 30.8%
P_{BL}	Out of band blocking		4		dBm	30 MHz to 2000 MHz
	Out of band blocking		-7		dBm	2003 MHz to 2399 MHz
	Out of band blocking		-7		dBm	2484 MHz to 2997MHz
	Out of band blocking		4		dBm	3000 MHz to 12.75 GHz
P_{INT}	Intermodulation		-32		dBm	
F_{ET}	Frequency error tolerance		+/- 125		kHz	
AC Characteristics - Tx						
Pout	Peak output power level	-20	0	+6	dBm	
Pout_step	Power control step		0.5		dB	
$P_{OUT,VAR}$	Average Tx output power variance between channels		+/- 0.5		dB	
Pout_HD2	Second harmonic output power level		-40		dBm	
Pout_HD3	Third harmonic output power level		-40		dBm	
Pout_HD4	Fourth harmonic output power level		-40		dBm	
DEV_{1Mbps}	1Mbps data rate frequency deviation	225	250	275	kHz	
DEV_{2Mbps}	2Mbps data rate frequency deviation	450	500	550	kHz	
32MHz Crystal Oscillator						
F_{XTAL}	Crystal frequency		32		MHz	
ΔF_{XTAL}	Frequency tolerance	-40		+40	ppm	Untrimmed;

						include initial tolerance/aging/temperature drift
C_L	Crystal load capacitance	6	8	12	pF	
ESR	Equivalent serial resistance			100	ohm	
T_{XTAL}	Startup time		0.35	1	ms	
32MHz RC Oscillator						
F_{RCH}	Frequency		32		MHz	
FAU_{RCH}	Untrimmed frequency accuracy	-8		+8	%	
FAC_{RCH}	Trimmed frequency accuracy	-1.5		+1.5	%	
T_{RCH}	Startup time		10		us	
32.768kHz Crystal Oscillator						
F_{XTAL}	Crystal frequency		32.768		kHz	
ΔF_{XTAL}	Frequency tolerance	-250		+250	ppm	Untrimmed; include initial tolerance/aging/temperature drift
C_L	Crystal load capacitance		7		pF	
T_{XTAL}	Startup time		500		ms	
32kHz RC Oscillator						
F_{RCL}	Frequency		32		kHz	
FAU_{RCL}	Untrimmed frequency accuracy	-8		+8	%	
FAC_{RCL}	Trimmed frequency accuracy	-0.2		+0.2	%	
T_{RCL}	Startup time		300		us	
SPI						
F_{SCK}	SPIS Clock Frequency			16	MHz	
DC-DC						
IND	DC-DC Inductor		2.2		uH	
C_{OUT}	DC-DC Capacitor		1		uF	

η	Efficiency		85	90	%	10mA loading
REG_{LINE}			0.7		%/V	1.62 ~ 3.63V
REG_{LOAD}			-0.02		%/mA	
V_{Ripple}	Ripple Voltage		5		mV	
IO						
V_{IH}	DC-DC Inductor		2.2		uH	
VIL	DC-DC Capacitor		1		uF	
VOH	Loading = 8mA		2.68	VCC	V	
	Loading = 4mA		2.72	VCC	V	
VOL	Loading = 8mA	0	0.33		V	
	Loading = 4mA	0	0.28		V	
I_{PU}	Pull up current	50			uA	
I_{PD}	Pull down current	50			uA	

5. Power Mode

To minimize power consumption, NS8803 supports a number of power modes and power management features as below.

Table 5: Power Mode

Block		POWER MODE				Reset MODE
		Active	Idle	Standby	Sleep	
CPU		Active	Halt	Off	Off	Off
RAM		Retention	Retention	Retention	Partial	Off
RF		Active Available	Active Available	Off	Off	Off
CLOCK	XO32M	Active	Active	Active	Off	Off
	RC32M	Active Available	Active Available	Active Available	Off	Off
	XO32K	Active Available	Active Available	Active Available	Active Available	Off
	RC32K	Active Available	Active Available	Active Available	Active Available	Off
Peripheral Interface		Active Available	Active Available	Off	Off	Off
Wake UP	Timer	Active Available	Active Available	Active Available	Active Available	Off
	Wakeup PIN (SPIS CSN)	Active Available	Active Available	Active Available	Active Available	Off
	RESETN	Active Available	Active Available	Active Available	Active Available	Active Available
Time to Active		—	5μs	25μs	1ms	1ms

6. Clocking

NS8803 supports crystal clock and single-ended clock sources. In the case where NS8803 is stand-alone. A 32MHz and 32kHz crystal is required. The 32MHz crystal is connected to the XO32MP and XO32MM pins as shown below. The 32KHz crystal is connected to the XO32KP and XO32KM pins as shown below.

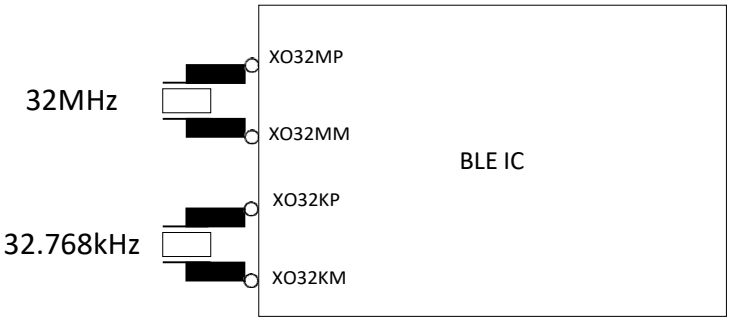

Figure 2: NS8803 Crystal Oscillators

When coupled with Apollo4 MCU, the clocks are sourced from the MCU to NS8803. In this configuration, the 32MHz clock is driven on XO32MP as a single-ended signal. The 32kHz clock is driven on XO32kP as a single-ended signal. The CLKREQ and CLKACK signals are used to drive clock request and acknowledge to and from the MCU. This allows the MCU to power down the high frequency crystal to save power. CLKACK is not connected in NS8803 as there is clock detection circuit in the design.

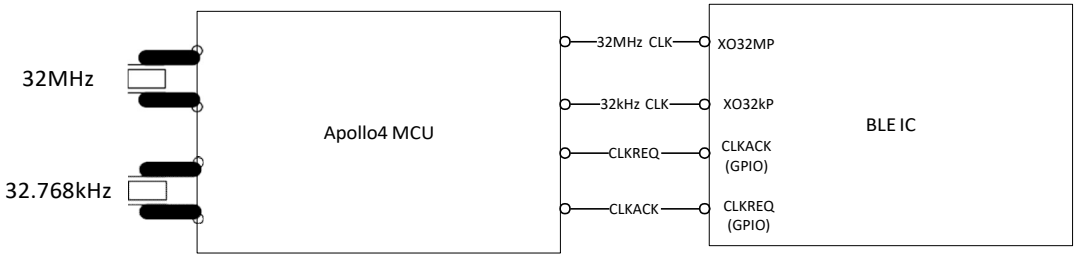

Figure 3: Apollo4/NS8803 Clocking Interface

NS8803 has an integrated PLL for generating the high frequency clocking required for the 2.4GHz radio. When companion to the Apollo4 MCU, the MCU supplies the clocks to NS8803. The low frequency clock is always running when interfaced with NS8803. The high frequency clock is disabled when not needed. The clock is enabled/disabled based on a request from NS8803.

7. Timing Requirement

1. RESETN is active low. When RESETN becomes 0, NS8803 goes to reset state. When RSTN rises up, NS8803 goes to active state after at least 1ms.

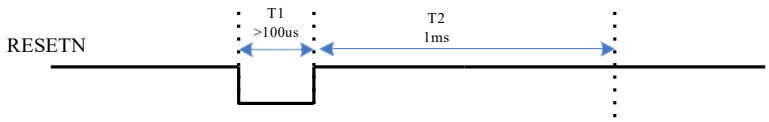

Figure 4: RESETN timing

2. SPIS can only support mode 3.

8. Integration Guidelines

1) Bonding wires for RFIOP and RFIOM should be as short as possible, good to be less than 1mm;
2) Do not need to bond DVDD and VDDPA. These two can be used for test;
3) Do not need to bond CMS0_PAD and CMS1_PAD;
4) Connect VSSESD pads as many as possible for better ESD performance;
5) Left open those unnecessary interfaces if they are not used;
6) For VCCESD pads, only need to connect No. 46 besides RESETN. The others can be left open;
7) Bond XO32MP_test to XO32MP in single-ended clocking case

9. Application Information

Very few external components are required for the operation of NS8803. This section provides an example of application circuits with schematic. External matching network is optional because the impedance at the RFIO port is designed to be 50ohm. External decouple capacitor is needed to suppress noise for sensitive RF circuits. This capacitor should be placed close to the main power supply of NS8803 which is VDCDC and VDCDCRF on the below diagram. Default data exchange interface is SPI. It is easy for integration with Host MCU and debug use.

For single-ended clocking from Apollo4 or other clock source, XO32MP and XO32kP are the input ports. Use CLKREQ as companion signal.

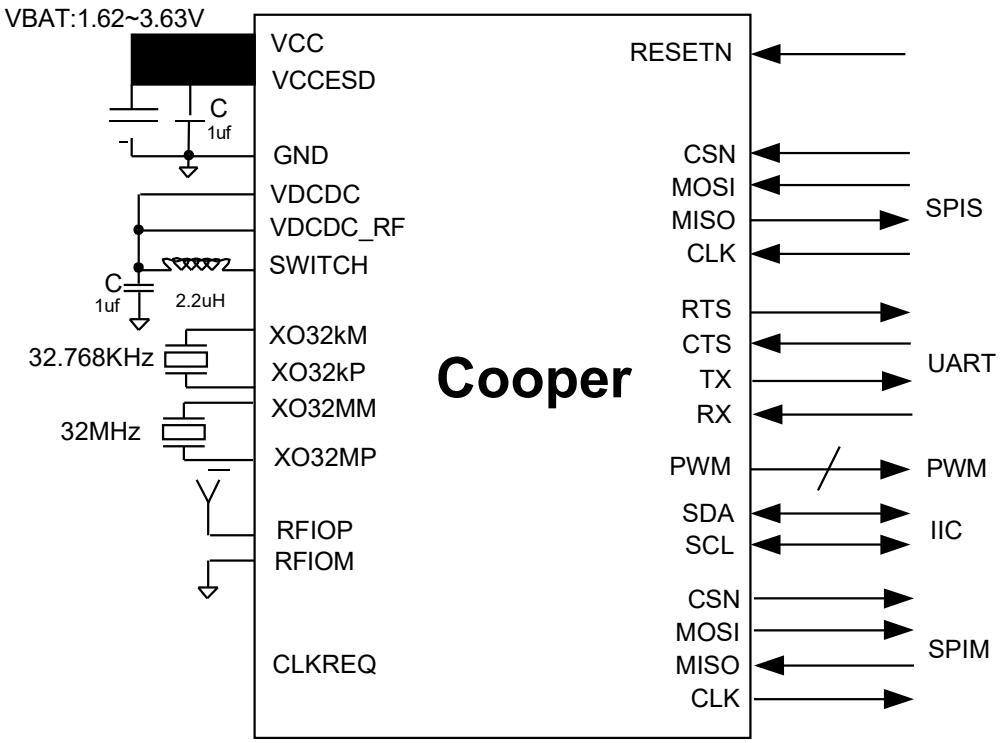

Figure 5: Application diagram